AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) An asynchronous data transmitting apparatus, comprising:

a first transmission line having a first delay;

a second transmission line having a ~~second~~ delay smaller than the first delay;

a third transmission line having a ~~second~~ delay larger than the first delay;

a transmitter that includes

a first transmitting unit that transmits a data signal through the first transmission line, ~~depending on~~ in accordance with a first clock;

a second transmitting unit that transmits a control signal through the second transmission line, ~~depending on~~ in accordance with the first clock; and

a third transmitting unit that transmits the control signal through the third transmission line, ~~depending on~~ in accordance with the first clock; and

a receiver that includes

a clock generator that generates a second clock from the control signals transmitted through the second and third transmission ~~line~~ lines, wherein a pulse of the second clock is provided in a period from a first pulse-edge of the control signal transmitted through the third transmission line to a second pulse-edge subsequent to the first pulse edge, the second pulse-edge being of the control signal transmitted through the second transmission line; and

a data receiving unit that receives the data signal through the first transmission line, ~~depending on~~ in accordance with the second clock.

2. (Original) The asynchronous data transmitting apparatus according to claim 1, wherein

the control signal has two binary levels which alternate in each transmission cycle.

3. (Currently Amended) The asynchronous data transmitting apparatus according to claim 1, wherein

the clock generator includes

a first unit that outputs a suppressing signal during a period when logic levels of the control signals do not coincide; and

a second unit that generates the second clock, in response to an end of the suppressing signal, ~~depending on~~ in accordance with a third clock.

4. (Original) The asynchronous data transmitting apparatus according to claim 3, wherein

the first unit is an EXNOR circuit~~gate~~ to which the control signals transmitted through the second and third transmission lines are input, and the EXNOR circuit~~gate~~ outputs the suppressing signal, and

the second unit is an AND circuit~~gate~~ to which the suppressing signal and the third clock, and the AND circuit~~gate~~ outputs the second clock.

5. (Original) The asynchronous data transmitting apparatus according to claim 1, wherein

the control signal is the first clock.

6. (Original) The asynchronous data transmitting apparatus according to claim 3, wherein

the first unit is a NAND circuit~~gate~~ to which the control signal transmitted through the second transmission line and an inversion of the control signal transmitted through the third transmission line are input, and the NAND circuit~~gate~~ outputs the suppressing signal, and

the second unit is an AND circuit~~gate~~ to which the suppressing signal and the third clock, and the AND circuit~~gate~~ outputs the second clock.

7. (Currently Amended) An asynchronous data transmitting apparatus, comprising:

a first transmission line having a first delay;

a second transmission line having a ~~second~~ delay smaller than the first delay;

a third transmission line having a ~~second~~ delay larger than the first delay;

a transmitter that includes

a first transmitting unit that transmits a data signal through the first transmission line, ~~depending on~~ in accordance with a first clock;

a second transmitting unit that transmits a control signal through the second transmission line, ~~depending on~~ in accordance with the first clock; and

a third transmitting unit that transmits the control signal through the third transmission line, ~~depending on~~ in accordance with the first clock; and

a receiver that includes

a data receiving unit that receives the data signal through the first transmission line, ~~depending on~~ in accordance with a second clock; and

a processing unit that generates an enable signal from the control signals transmitted through the second and third transmission line, and determines whether to read the received data signal ~~received~~ based on the enable signal, wherein a pulse of the second clock is provided in a period from a first pulse-edge of the control signal transmitted through the third transmission line to a second pulse-edge subsequent to the first pulse edge, the second pulse-edge being of the control signal transmitted through the second transmission line.

8. (Original) The asynchronous data transmitting apparatus according to claim 7, wherein

the control signal has two binary levels which alternate in each transmission cycle.

9. (Currently Amended) The asynchronous data transmitting apparatus according to claim 7, wherein

the processing unit includes

a first unit that outputs a suppressing signal during a period when logic levels of the control signals do not coincide; and

a second unit that generates the enable signal, in response to an end of the suppressing signal, ~~depending on~~ in accordance with the second clock.

10. (Currently Amended) The asynchronous data transmitting apparatus according to claim 9, wherein

the first unit is an EXNOR circuit~~gate~~ to which the control signals transmitted through the second and third transmission lines are input, and the EXNOR circuit~~gate~~ outputs the suppressing signal, and

the second unit is a flip flop to which the suppressing signal is input ~~depending on~~ in accordance with the second clock, and the flip flop circuit~~gate~~ outputs the enable signal.

11. (Original) The asynchronous data transmitting apparatus according to claim 7, wherein

the control signal is the first clock.

12. (Currently Amended) An asynchronous data transmitting apparatus, comprising:

a first transmission line having a first delay;

a second transmission line having a second delay;

a transmitter that includes

a first transmitting unit that transmits a data signal through the first transmission line, ~~depending on~~ in accordance with a first clock; and

a second transmitting unit that transmits a control signal through the second transmission line, ~~depending on~~ in accordance with the first clock; and

a receiver that includes

a clock generator that generates a second clock from the control signal transmitted through the second transmission line; and

a data receiving unit that receives the data signal through the first transmission line, depending on the second clock;

wherein the transmitter is configured to transmit asynchronous data in a system in which the first clock and the second clock are generated independently of one another, and the timing of reading received data is controlled based on information of the first clock.

13. (Original) The asynchronous data transmitting apparatus according to claim 12, wherein

the control signal has two binary levels which alternate in each transmission cycle.

14. (Original) The asynchronous data transmitting apparatus according to claim 12, wherein

the control signal is the first clock.

15. (Original) The asynchronous data transmitting apparatus according to claim 12, wherein

the clock generator includes

an inverter that inverts the control signal transmitted through the second transmission line and outputs a suppressing signal; and

an AND circuit~~gate~~ to which the suppressing signal and a third clock, wherein the AND circuit~~gate~~ outputs the second clock.

16. (Original) The asynchronous data transmitting apparatus according to claim 12, wherein

the clock generator includes

an AND circuit~~gate~~ to which the control signal transmitted through the second transmission line and a third clock, wherein the AND circuit~~gate~~ outputs the second clock.

17. (Original) The asynchronous data transmitting apparatus according to claim 12, wherein

the second delay is smaller than the first delay;

the clock generator generates the second clock from the control signal transmitted through the second transmission line and a delayed signal, wherein

the delayed signal is delayed by a predetermined delay from a leading edge of the control signal, the predetermined delay is not less than a difference between the first delay and the second delay, and

a pulse of the second clock is provided in a period from a leading edge of the delayed signal to a leading edge of the control signal transmitted through the second transmission line.

18. (Currently Amended) The asynchronous data transmitting apparatus according to claim 17, wherein

the clock generator includes

a delay unit that generates the delayed signal from the control signal transmitted through the second transmission line;

a NAND circuit~~gate~~ to which the control signal transmitted through the second transmission line and an inversion of the delayed signal are input, wherein the NAND circuit~~gate~~ outputs a suppressing signal; and

an AND circuit~~gate~~ to which the suppressing signal and a third clock are input, wherein the AND circuit~~gate~~ outputs the second clock.

19. (Original) The asynchronous data transmitting apparatus according to claim 12, wherein

the second delay is larger than the first delay;

the clock generator generates the second clock from the control signal transmitted through the second transmission line and a delayed signal, wherein

the delayed signal is delayed by a predetermined delay from a leading edge of the control signal, the predetermined delay is not more than a difference between the first delay and the second delay, and

a pulse of the second clock is provided in a period from a leading edge of the control signal transmitted through the second transmission line to a trailing edge of the delayed signal.

20. (Original) The asynchronous data transmitting apparatus according to claim 19, wherein

the clock generator includes

a delay unit that generates the delayed signal from the control signal transmitted through the second transmission line;

an OR circuit to which the control signal transmitted through the second transmission line and the delayed signal are input, wherein the OR circuit outputs a suppressing signal; and

an AND circuit to which the suppressing signal and a third clock, wherein the AND circuit outputs the second clock.